Laboratory 1

(Due date: **002/003/008**: Sep. 21st, **004/011/013/016**: Sep. 22nd, **005**: Sep. 23rd, **007**: Sep. 24th, **012/014**: Sep. 25th)

OBJECTIVES

✓ Introduce VHDL Coding for FPGAs.
✓ Learn to write testbenches in VHDL.
✓ Learn the Xilinx FPGA Design Flow with the Vivado HL: Synthesis, Simulation, and Bitstream Generation.
✓ Learn how to assign FPGA I/O pins and download the bitstream on the Nexys™ A7-50T Board.

VHDL CODING

✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

NEXYS™ A7-50T FPGA TRAINER BOARD SETUP

▪ The Nexys A7-50T Board can receive power from the Digilent USB-JTAG Port (J6). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
▪ Nexys A7-50T documentation: Available in class website.

FIRST ACTIVITY (100/100)

DESIGN PROBLEM

▪ A lock is opened ($f=1$) only for five combinations of four switches: 0001, 0100, 1011, 1100, 1111, where '1' represents the ON state of the lock and '0' the OFF state. The state of the switches is represented by the Boolean variables a, b, c, d.

a	b	c	d	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

✓ Complete the truth table for this circuit: (5 pts)

✓ Derive (simplify if possible) the Boolean expression: (10 pts)

$f =$

PROCEDURE

▪ **Vivado Design Flow for FPGAs: complete the following steps (follow the order <u>strictly</u>)**: (85 pts)

✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device as per the table:

Kit	Artix-7 FPGA Device	Master XDC File	Comments
Nexys A7-50T	XC7A50T-1CSG324I	Nexys-A7-50T-Master.xdc	Recommended board.
Nexys A7-100T	XC7A100T-1CSG324C	Nexys-A7-100T-Master.xdc	
Basys 3	XC7A35T-1CPG236C	Basys-3-Master.xdc	Suggested if you only take ECE2700
Nexys 4 Nexys 4 DDR	XC7A100T-1CSG324C	Nexys4_Master.xdc Nexys4DDR_Master.xdc	Discontinued

✓ Write the VHDL code that implements the simplified Boolean expression. Synthesize your circuit (Run Synthesis).

✓ Write the VHDL testbench to test every possible combination of the inputs.
  ▫ The figure below provides a suggestion of what the input waveform described by your testbench should look like. Complete the output f so that you can compare it with the output generated by the simulator (next step).
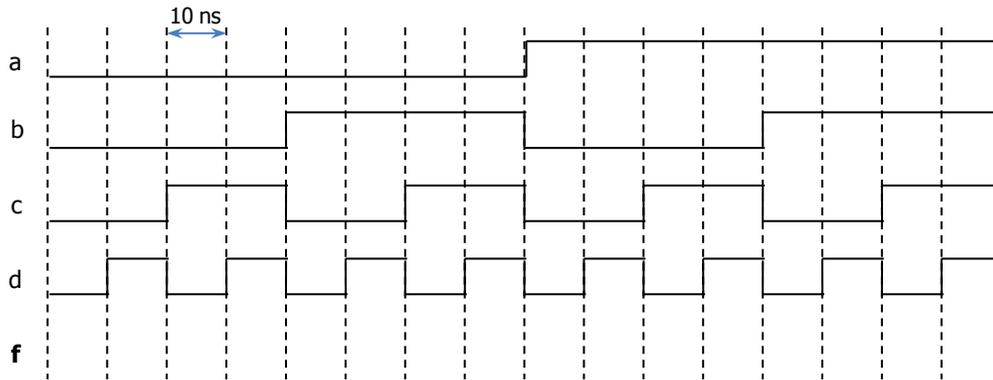
✓ Perform <u>Functional Simulation</u> (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your TA.**

✓ I/O Assignment: Generate the XDC file. Download the corresponding constraints file (XDC) of your board and edit it.
  ▫ Use `SW3`, `SW2`, `SW1`, `SW0` as inputs a, b, c, d respectively. Use `LED0` as the output f.
  ▫ The board pin names (`SW0-SW3`, `LED0`) are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.

✓ Implement your design (Run Implementation).

✓ Do <u>Timing Simulation</u> (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**

✓ Generate the bitstream file (Generate Bitstream).

✓ Download the bitstream on the FPGA (Open Hardware Manager) and test. **Demonstrate this to your TA.**

▪ Submit (<u>as a .zip file</u>) the generated files: VHDL code, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____   **Date:** _____